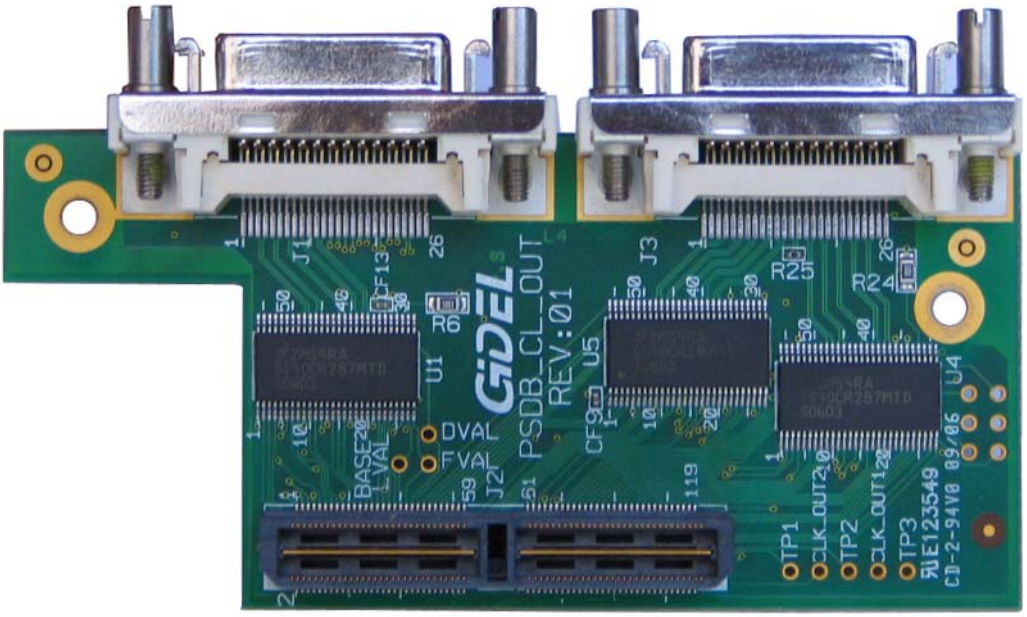
PSDB_CL_OUT™

CameraLink Transmitter Daughter Board



Data Book

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Contents

Figures and Table

Introduction

GiDEL PROCStar II™ and ***GiDEL PROCSpark II™*** boards were designed to work with daughterboards. A number of connectors located on the component side of the PROC motherboards enable connecting several daughterboards to these motherboards. These daughter boards are called **PSDB**. PSDBs can be used for system adaptation and to add logic.

There are two types of PSDB: **PSDB1** and **PSDB2**.

- **PSDB1** (PSDB of type 1) provide a convenient means to connect external signals to the PROC motherboard via buffers / transceivers located on the daughterboard.

- **PSDB2** (PSDB of type 2) may be used to provide several functions:

    - Adding unique features, such as DSPs, to the motherboard
    - Adding massive and fast connections to the FPGAs

PSDB_CL_OUT™ is a PSDB of type 1. This means that it uses a single connector to connect to the PROC motherboard. On PROC boards, this connector is located to the left of the target FPGA.

PSDB_CL_OUT™ is designed to provide a CameraLink connection to the PROC motherboard via its panel.

Key Features

GiDEL PSDB_CL_OUT™ provides a simple and convenient way to simulate CameraLink video data with ***GiDEL PROCStar II™*** and ***PROCSpark II™*** boards.

PSDB_CL_OUT™ key features include:

- ✓ Support of standard CameraLink modes (base, medium, full)
- ✓ Serial Communication with receiver device
- ✓ Simple interface
- ✓ Automatic detection by hardware / software
- ✓ Designed to work with ***GiDEL PROCCamLink™*** Simulator IP*
- ✓ Automatic integration of ***GiDEL PROCCamLink™*** Simulator IP into user's top-level design using ***GiDEL PROCWizard™***

**** Check availability with GiDEL***

PSDB_CL_OUT™ uses two MDR 26-pin female connectors (**J1** and **J3**), according to CameraLink standards.

The following adapters are used in ***PSDB_CL_OUT™*** to convert the CameraLink Signals:

- ➤ National Semiconductor **DS90CR287MTD/NOPB** for LVTTL to LVDS data signal conversion.
- ➤ National Semiconductor **DS90LV047ATMTC/NOPB** for LVDS CMOS DIFFERENTIAL Driver control signal conversion.
- ➤ National Semiconductor **DS90LV019TMTC/NOPB** for LVDS Driver Receiver serial control signal conversion.

Locations

PROCStar II™ and ***PROCSpark II***™ motherboards have a number of connectors that allow different installation options for ***PSDB_CL_OUT***™ daughterboards. The following figure shows installation options when using a PROCStar II motherboard.

Since ***PSDB_CL_OUT***™ is a PSDB of type 1, it is connected to the target FPGA via a single connector. This connector is always located on the board's component side to the left of the target FPGA. For example, placing ***PSDB_CL_OUT***™ on connector **J7** on a PROCStar II motherboard in location1 connects that daughterboard to **IC1**.

For mechanical reasons location 1(connector **J7**) is the preferred site on which to place the daughterboard. Nevertheless, it will work properly when connected to any other location on the PROC board.

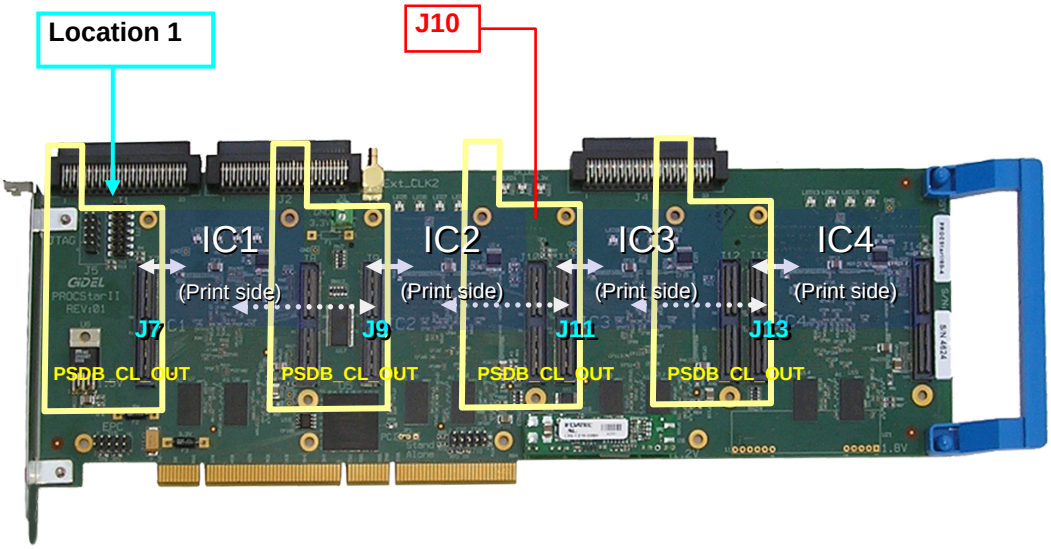

Figure 1: ***Possible Locations of PSDB_CL_OUT***™

The terms **FPGA right side** and **FPGA left side** should be treated as if the FPGAs and the connectors are on the same side and viewed as shown above. For example, **J9** is the left connector of **IC2** and **J10** the right connector of **IC2**.

PSDB boards of type 1 are installed on odd-numbered connectors **J7** to **J13**.

Important

Connecting *PSDB_CL_OUT*™ to an even-numbered connector (J8 to J14), may damage the daughterboard. Always check for correct positioning of the daughterboard on the PROC motherboard!

The FPGA devices and connectors are located on opposite sides of GiDEL PROC boards and connecting a daughter board will not hinder the FPGAs' cooling.

It is possible to connect several different types of daughterboards to a PROC motherboard.

Connections

CameraLink transmission method requires only a small number of conductors to transfer data. Using this method, five pairs of LVDS wires can transmit up to 28 bits of data.

***PSDB_CL_OUT*™** has two connectors used for CameraLink communication: **J1** and **J3**.

J1 is connected to five twisted pairs of LVDS wires that transport the **Base** mode CameraLink signals. In addition, two twisted pairs of LVDS wires provide serial communication with the camera and four additional twisted pairs are used for camera control.

J3 is used for **Medium** and **Full** modes. Five twisted pairs of LVDS wires transport the **Medium** mode signals and another five twisted pairs transport the **Full** mode signals.

Important

Warning: J1 and J3 must be carefully connected to the system. Swapping J1 and J3 may damage the PROC motherboard and the daughterboard, as well as the external device (camera).

Please, refer to CameraLink specification for detailed explanations about the connectors' pinout.

CameraLink I/Os

The following table describes the signals and buses as they appear in the top-level design generated by ***GiDEL PROCWizard***.

Symbol	Function	Direction
txout_base_clk	Base output clock (CLKX).	Output
txout_base[27..0]	CameraLink data. Base data	Output
txout_medium_clk	Medium output clock (CLKY).	Output
txout_medium[27..0]	CameraLink data. Medium data	Output
txout_full_clk	CameraLink data. Full output clock (CLKZ).	Output
txout_full[27..0]	CameraLink data. Full data	Output
cc_in[4..1]	General-purpose camera control lines	Input
en	Camera Control lines receiver enable: 1: Enable. 0: Disable	Input
din	Serial comm. data (TX).	Output
de	Serial (TX) Driver Enable. 1: Enable. 0: Disable	Output
rout	Serial comm. data (RX).	Input
re	Enable for serial comm. (RX) , active LOW 0: Enable. 1: Disable	Output

Table 1 : CameraLink I/Os

Mechanical Specifications

***PSDB_CL_OUT*™** is a **PSDB1** type daughterboard and its mechanics are compliant to PSDB1 mechanical description. A top view is seen below.

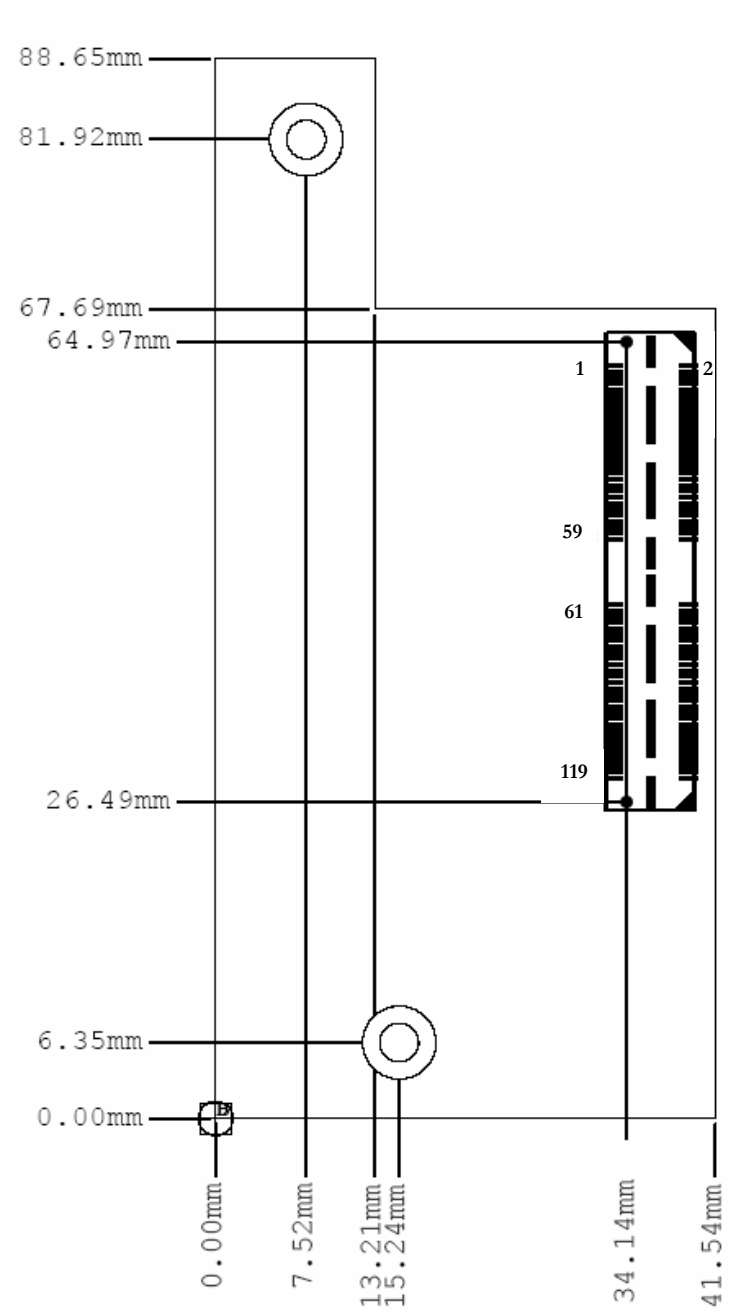

Figure 2: *PSDB_CL_OUT*™ Mechanical Dimensions