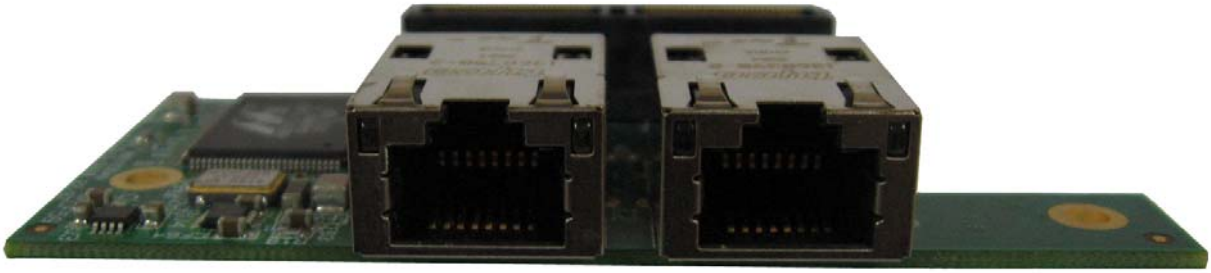
PSDB_PHY2

1 Gbps Switched Ethernet Networking Daughterboard



Data Book
January 2009

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Introduction

The GiDEL line of ***PROC*** boards provide a high capacity, high-speed FPGA-based platform equipped with high throughput and massive memory resulting in a powerful and highly flexible system. These PROC boards are designed to support GiDEL daughter boards (**PSDB**s) enabling to connect external IO lines, to add unique features, and to expand the FPGA's connectivity.

The ***GiDEL PSDB_PHY2***™ daughter board enables to add to a PROC board two switched RJ45 copper ports for 1Gbps Ethernet networking.

The Gidel PSDB family includes two types of daughter boards referred to as **PSDB1** and **PSDB2**, each composed of single and dual connectors, respectively. The ***PSDB_PHY2*** is a PSDB1 type daughter board. To determine if your PROC board supports PSDB1 daughter board, contact the Gidel technical support.

Key Features

The following figure shows a block diagram of the ***PSDB_PHY2*** system.

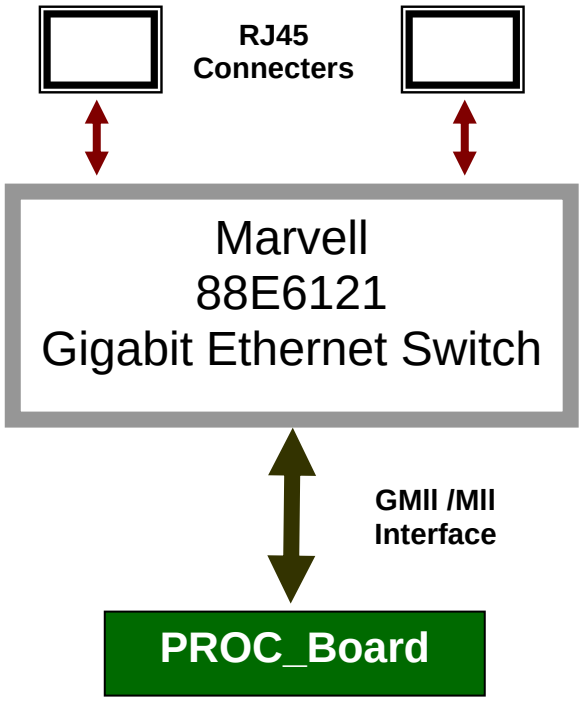

Figure 1 : *PSDB_PHY2*™ block diagram.

GiDEL PSDB_PHY2 includes the following features:

- ✓ Two switched 1Gbps RJ45 copper Ethernet ports
- ✓ Marvell 88E6121 Gigabit Ethernet Switch
- ✓ GMII/MII MAC interface from switch to FPGA.
- ✓ FPGA Switch management
- ✓ Automatic detection by hardware / software

Standard Models

The following model is currently available:

Ordering Code (Basic Model)	Switch Device	Number of Ports
PSDB_PHY2™	88E6121	2

Table 1: *PSDB_PHY2*™ Standard Models

The *GiDEL PROCWizard*™ software can generate a top-level design for each FPGA located on a PROC board. For an FPGA connected to ***PSDB_PHY2***, the ***PROCWizard*** automatically generates the top-level signals that connect to the ***PSDB_PHY2*** switches. The ***PROCWizard*** also generates the board constrains needed to physically connect these signals to the daughterboard.

The following figure shows the ***PSDB_PHY2*** and PROC board FPGA signal connectivity:

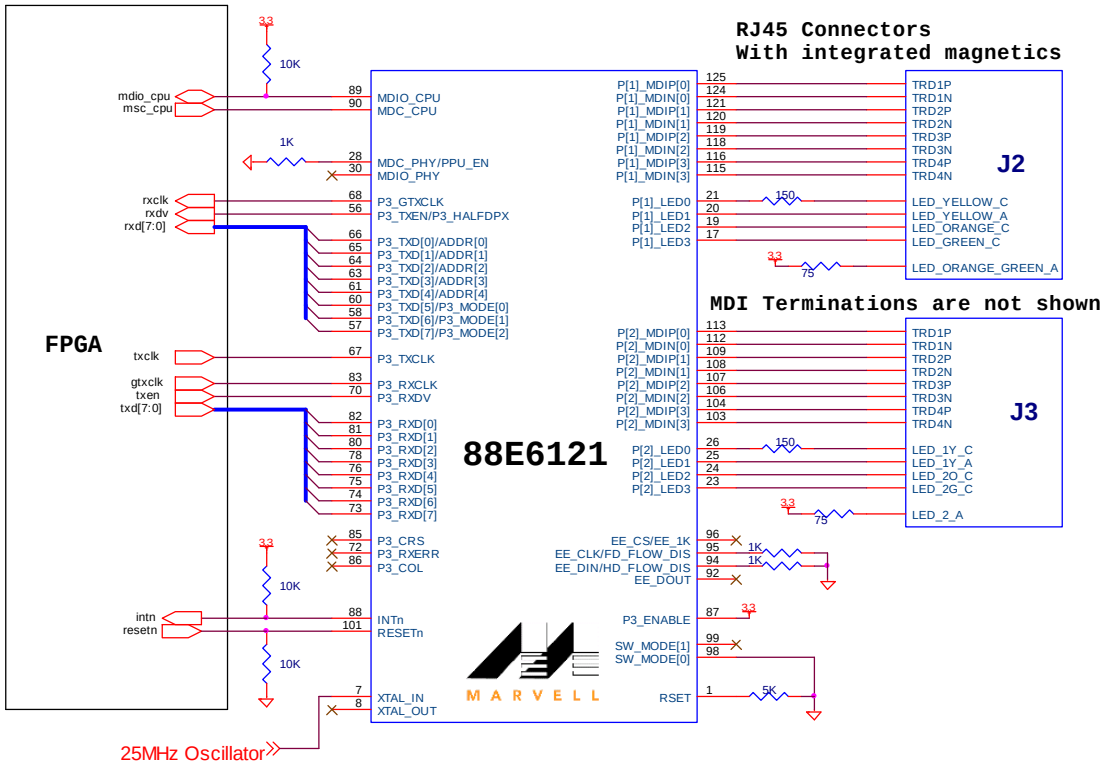

Figure 2: PSDB_PHY2 Signal Connectivity Schematic

The following table describes the generated top-level signals and their functions.

Symbol	Function	Direction
mdc_cpu	**MDC** is the clock reference for the serial management interface. A continuous clock stream is not mandatory. The maximum frequency supported is 8.3 MHz. **MDC** for the designated port must be left floating when not used.	Output
mdio_cpu	**MDIO** is the management data. MDIO transfers management data in and out of the device synchronously to MDC. If not used, this signal must be set as "Z".	In/Out
resetn	**Switch Hardware Reset**. Active low.	Output
rxclk	**Receive Clock**. RXCLK provides a: • 125 MHz clock reference for RXDV and RXD[7..0] in 1000Mbps mode • 25 MHz clock reference in 100 Mbps mode • 2.5 MHz clock reference in 10 Mbps mode.	Input
rxdv	**Receive Data Valid**. When RXDV is asserted, data received on the cable is decoded and presented on RXD[7..0]. RXDV is synchronized to RXCLK.	Input
rxd[7..0]	**Receive Data**. Symbols received on the cable are decoded and presented on: • RXD[7..0] in 1000Mbps mode • RXD[3..0] in 10/100Mbps modes. RXD[7..4] is driven low in these modes. RXD[7..0] is synchronized to RXCLK.	Input
txen	**Transmit Enable**. When TXEN is asserted, data on TXD[7..0] is encoded and transmitted onto the cable. TXEN is synchronous to GTXCLK in 1000 Mbps mode and synchronous to TXCLK in 10/100Mbps modes.	Output

Symbol	Function	Direction
txclk	**MII Transmit Clock**. TXCLK provides a: • 25 MHz clock reference for TXEN, TXER, and TXD[3..0] in 100Mbps mode • 2.5 MHz clock reference in 10Mbps mode. Not used in GMII mode.	Input
txd[7..0]	**Transmit Data**. In GMII mode, TXD[7..0] presents the data byte to be transmitted onto the cable in 1000Mbps mode. In MII mode, TXD[3..0] presents the data nibble to be transmitted onto the cable in 10/100Mbps modes. TXD[7..4] is ignored in these modes, but must be driven either high or low. TXD[7..0] is synchronized to GTXCLK in 1000Mbps mode and synchronized to TXCLK in 10/100Mbps modes.	Output
gtxclk	**GMII Transmit Clock**. GTXCLK provides a 125 MHz clock reference for TXEN and TXD[7..0]. This clock can be stopped when the device is in 10/100Mbps modes, and during Auto-Negotiation.	Output
intn	**Interrupt From Switch**. Active low	Input

Table 2: User I/Os

Mechanical Specifications

PSDB_PHY2 is a PSDB type 1 daughterboard in accordance to the following mechanical dimensions:

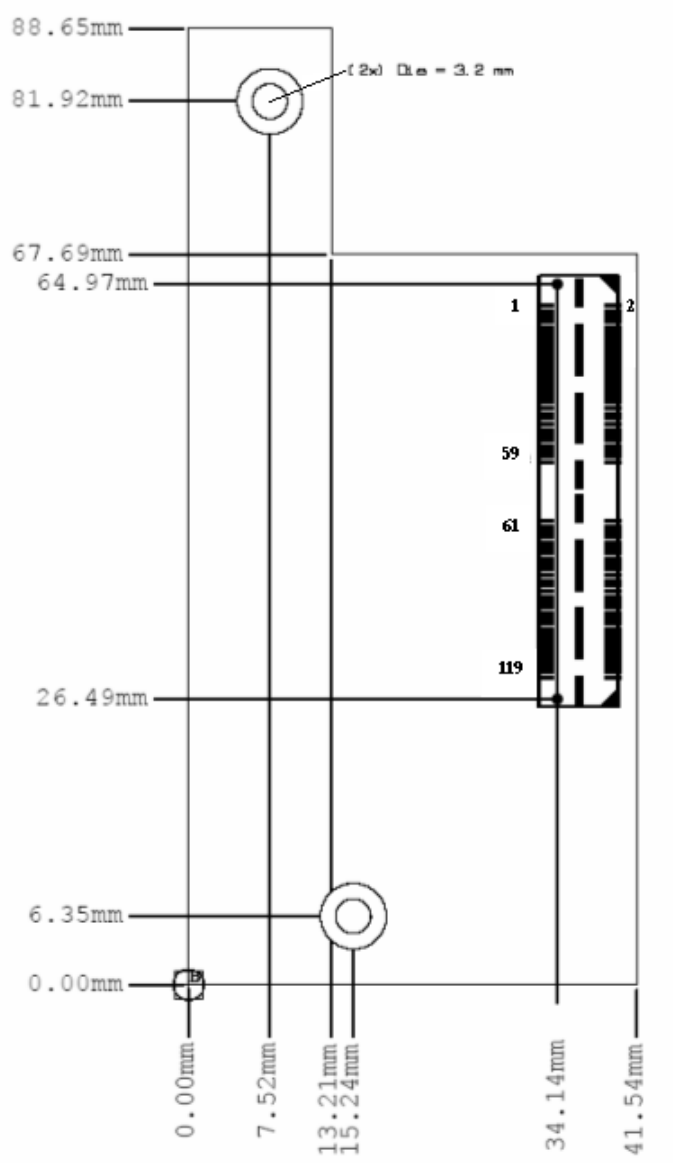

Figure 3 : *PSDB_PHY2*™ Mechanical Dimensions (bottom view).

Power Consumption

PSDB_PHY2 obtains its power from the motherboard's 3.3 Volt source

The following table describes the ***PSDB_PHY2*** current consumption.

Minimum	Maximum
0.5A	1.5A

Table 3: *PSDB_PHY2*™ Current Consumption

Note: The power consumption may vary depending on Ethernet link type and data rate.

Data Book History

Date	Changes
11/2006	Initial Version
01/2009	• Update of ***Table 2: User I/Os*** • Addition of ***Figure 2:PSDB_PHY2 Signal Connectivity Schematic***

Table 4: Data Book History